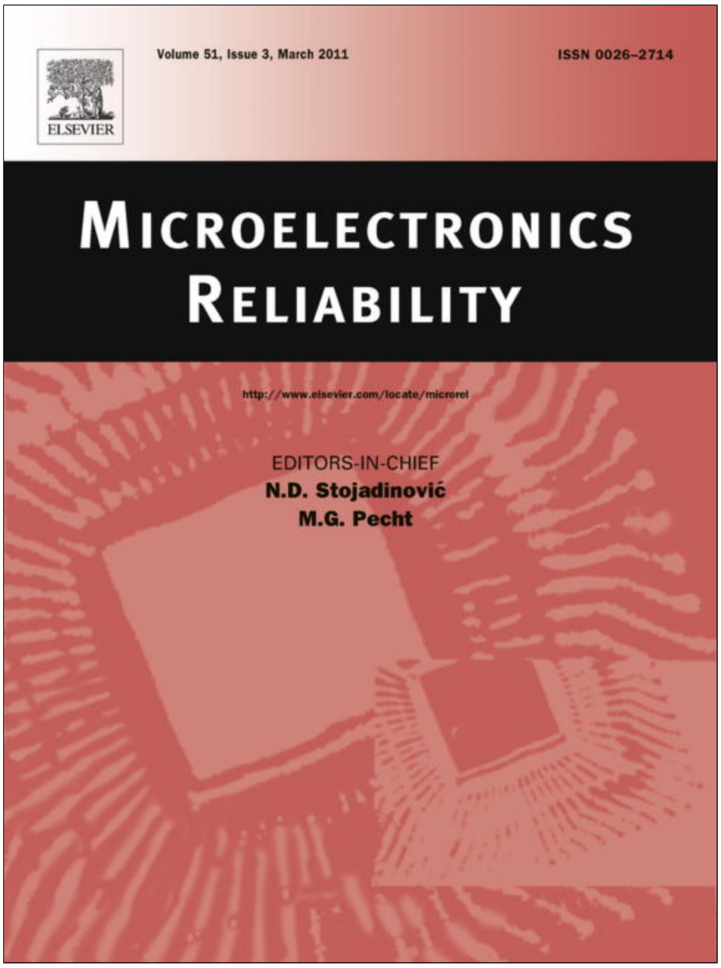
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Current transport mechanisms and trap state investigations in (Ni/Au)–AlN/GaN Schottky barrier diodes

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A B S T R A C T

The current transport mechanisms in (Ni/Au)–AlN/GaN Schottky barrier diodes (SBDs) were investigated by the use of current–voltage characteristics in the temperature range of 80–380 K. In order to determine the true current transport mechanisms for (Ni/Au)–AlN/GaN SBDs, by taking the $J_{s(\mathrm{tunnel})}$, E_0, and R_s as adjustable fit parameters, the experimental *J–V* data were fitted to the analytical expressions given for the current transport mechanisms in a wide range of applied biases and at different temperatures. Fitting results show the weak temperature dependent behavior in the saturation current and the temperature independent behavior of the tunneling parameters in this temperature range. Therefore, it has been concluded that the mechanism of charge transport in (Ni/Au)–AlN/GaN SBDs, along the dislocations intersecting the space charge region, is performed by tunneling.

In addition, in order to analyze the trapping effects in (Ni/Au)–AlN/GaN SBDs, the capacitance–voltage (*C–V*) and conductance–voltage (*G/ω–V*) characteristics were measured in the frequency range 0.7–50 kHz. A detailed analysis of the frequency-dependent capacitance and conductance data was performed, assuming the models in which traps are located at the heterojunction interface. The density (D_t) and time constants (τ_t) of the trap states have been determined as a function of energy separation from the conduction-band edge ($E_c - E_t$) as $D_t \cong (5\text{–}8) \times 10^{12}$ eV^{-1} cm^{-2} and $\tau_t \cong (43\text{–}102)$ µs, respectively.

1. Introduction

AlGaN/GaN heterostructures have attracted special interest due to their potential applications in high electron mobility transistors (HEMT) operating at high power and high temperature levels [1,2]. However, room temperature two-dimensional electron gas (2DEG) density and mobility in turn limit the sheet resistance of the channel and maximum HEMT current (1–1.5 A/mm) for AlGaN/GaN heterostructures [1]. Recently, the AlInN/GaN material system has attracted major interest for electronic applications due to its promising electronic properties, polarization effects, and high thermal stability [3]. AlInN/GaN heterostructures can further enhance the 2DEG density and lead to high HEMT current [3]. It was shown that the DC current levels in turn lead to 2.3 A/mm by using AlInN/AlN/GaN heterojunctions [4]. On the other hand, ultrathin all-binary AlN/GaN HEMTs with ultrathin AlN (2–5 nm) barriers offer higher sheet carrier density and a higher mobility 2DEG channel, which show much promise for high power, high temperature applications in telecommunications, power flow control, and remote sensing [5].

Both molecular-beam epitaxy (MBE) and metal organic chemical-vapor deposition (MOCVD) are currently used to grow high-quality AlGaN/GaN and AlInN/GaN heterostructures with excellent transport characteristics [1–6]. However, it is difficult to grow AlN/GaN HEMTs with high transport characteristics by an MOCVD reactor [7]. Alekseev et al. [8] reported on a low-pressure MOCVD technique for GaN/AlN heterojunction field-effect transistor growth. Room temperature electron mobility in an optimized structure with an 11 nm barrier was 320 cm^2/V s and the associated 2DEG density was 2.3×10^{13} cm^{-2}.

Because of the large mismatches in lattice constants and thermal expansion constants between GaN and all the available foreign substrates (Al_2O_3, SiC, ZnO, etc.) causes very high dislocation density (10^8–10^{10} cm^{-2}) in a hetero epitaxially grown crystalline GaN layer [2]. The high dislocation density constitutes a serious limitation for the efficiency of radiative recombination, and also for device performance and lifetime. Evstropov et al. [13] and Belyaev et al. [12] showed that the current flow in the III–V heterojunctions, with a high dislocation density, is commonly governed by multistep tunneling with the involvement of dislocations even at room temperature.

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In the present paper, we grow AlN/GaN HEMT structures in an MOCVD reactor and investigate the current transport mechanisms in a wide temperature range (80–380 K) in (Ni/Au)–AlN/GaN SBDs.

Another purpose of this paper is to characterize the density distribution and relaxation time of the interface states in AlN/GaN HEMT structures by using an admittance technique at room temperature.

2. Experimental

The AlN/GaN heterostructures were grown on c-plane (0 0 0 1) Al_2O_3 substrate in a low-pressure metalorganic chemical-vapor deposition (MOCVD) reactor by using trimethylgallium (TMGa), trimethylaluminum (TMAl), and ammonia for Ga, Al, and N precursors, respectively. The buffer structures consisted of high temperature (1150 °C) 840 nm AlN templates. A 1.6 μm nominally undoped GaN layer was grown on an AlN template layer at 1050 °C, which was followed by the growth of a 4 nm thick high temperature AlN (1150 °C) barrier layer. The ohmic and Schottky/rectifier contacts were made on top of the sample at approx. 10^{-7} Torr, respectively, within a high vacuum coating system. The ohmic contacts were formed as a square van der Pauw shape and the Schottky contacts were formed as 0.8 mm radius circular dots. After cleaning the samples, Ti/Al/Ni/Au (20/180/40/80 nm) metals were thermally evaporated on the sample and were annealed at 850 °C for 30 s in N_2 ambient in order to form the ohmic contact. Schottky contacts were formed by Ni/Au (50/80 nm) evaporation. Room temperature 2DEG density and mobility were found to be 2×10^{13} cm^{-2} and 485 cm^2/V s, respectively.

The current–voltage (*I*–*V*) measurements were performed by use of a Keithley 2400 SourceMeter. The frequency dependence of the *C*–*V* and *G*/*ω*–*V* measurements was obtained by using an HP 4192 A LF impedance analyzer. The measurements were performed under the sweep of bias voltage from ~(−6 V) to (+6 V) and a test signal of 40 mV peak to peak.

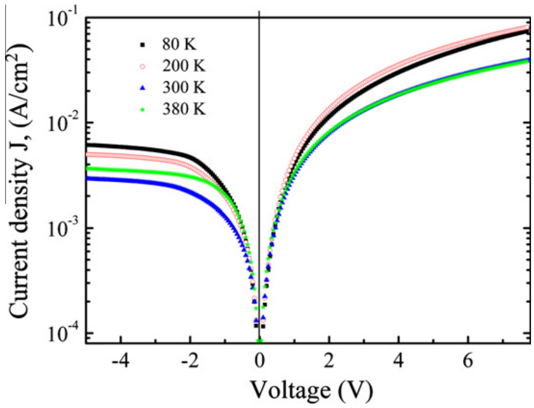

Fig. 1. The *J*–*V* characteristics of (Ni/Au)–AlN/GaN SBDs.

3. Results and discussion

The reverse and forward bias *I*–*V* characteristics of an (Ni/Au)–AlN/GaN SBDs were measured in a wide temperature range (80–380 K). In Fig. 1, the measured reverse and forward bias *J*–*V* characteristics of an (Ni/Au)–AlN/GaN SBDs for the temperatures of 80, 200, 300, and 380 K are given. In order to correctly interpret the current transport mechanisms in the (Ni/Au)–AlN/GaN SBDs, we considered the contribution of thermionic emission (TE) current and tunneling current transport mechanisms (see Fig. 2).

The forward bias *J*–*V* characteristics, due to thermionic emission (TE), of SBDs with the series resistance (R_s) is given by [9,10],

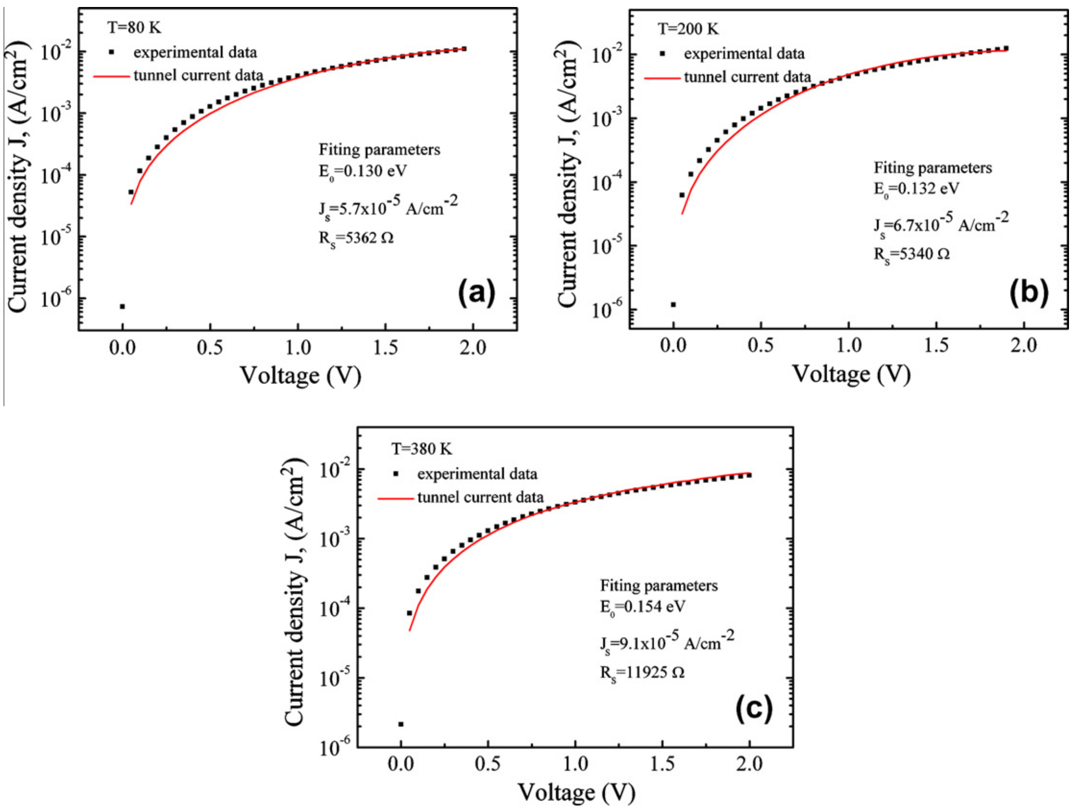

Fig. 2. The fitting of the tunneling current expression (Eq. (2)) to the experimental *J*–*V* characteristics of (Ni/Au)–AlN/GaN SBDs measured at 80, 200, and 380 K.

$$J_{\text{thermionic}} = J_{s(\text{thermionic})}\left\{\exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right\} \qquad (1)$$

where $J_{s(\text{thermionic})}$ is the reverse saturation current derived from the straight line region of the forward bias current intercept at a zero bias. T is the absolute temperature in K, q is the electron charge, n is the ideality factor, k is the Boltzmann constant, V is the applied bias voltage, and IR_s term is the voltage drop across the R_s of structure [9–11].

Table 1
Temperature dependent values of the tunneling saturation current density ($J_{s(\text{tunnel})}$), series resistance (R_s) determined by fitting expression as given in Eq. (2) to the measured forward bias J–V characteristics and the ideality factor (n) was determined from the semilog-forward J–V data set of (Ni/Au)–AlN/GaN SBDs.

T (K)	$J_{s(\text{tunnel})} \times 10^{-5}$ (A/cm^2)	n	R_s (Ω)
80	5.7	18.9	5362
110	5.9	13.6	5090
140	6.1	10.7	5290
170	6.4	8.8	4960
200	6.7	7.6	5340
230	7.1	6.8	5890
260	7.2	6.1	6782
290	7.6	5.7	8298
300	7.6	5.6	9015
320	7.8	5.4	10,274
340	8.4	5.2	11,020
360	8.7	4.9	11,241
380	9.1	4.7	11,923

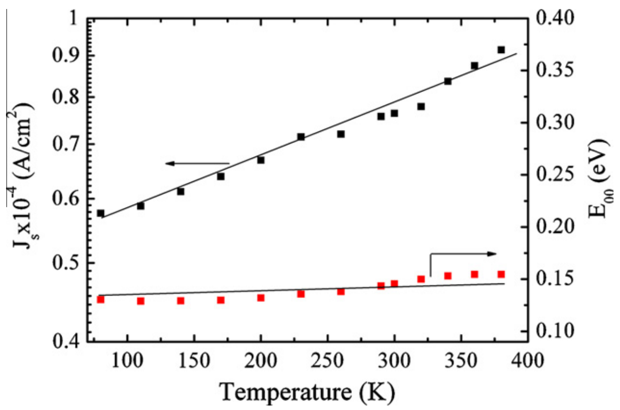

Fig. 3. The temperature dependences of the tunneling saturation current density ($J_{s(\text{tunnel})}$) and the characteristic energy of tunneling (E_{00}) for (Ni/Au)–AlN/GaN SBDs.

The values of ideality factor n were obtained from the slope of the linear region of the J–V plots [10,11]. The change in n with temperature is shown in Table 1. As shown in Table 1, the n determined from semilog-forward J–V plots were found to be a strong function of temperature. The ideality factor n was found to increase with decreasing temperature (n = 18.9 at 80 K, n = 4.7 at 380 K). It is obvious that the ideality factors of the structures are considerably larger than unity.

The tunneling current density through SBDs is given by [9–12],

$$J_{\text{tunnel}} = J_{s(\text{tunnel})}\left\{\exp\left[\frac{q(V-IR_s)}{E_0}\right]-1\right\} \qquad (2)$$

where $J_{s(\text{tunnel})}$ is the tunneling saturation current density and E_0 is the tunneling parameter. E_0 can be defined as [9–12],

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{kT}\right) \qquad (3)$$

where E_{00} is the characteristic tunneling energy that is related to the tunnel effect transmission probability. In order to determine the true current transport mechanisms for (Ni/Au)–AlN/GaN Schottky diodes, by taking the $J_{s(\text{tunnel})}$, E_0, and R_s as adjustable fit parameters, we fit the experimental J–V data to the analytical expressions given for the current transport mechanisms in a wide range of applied biases and at different temperatures. A standard software package was utilized for the curve fitting [10,11]. The tunneling saturation current ($J_{s(\text{tunnel})}$), tunneling parameter (E_0), and series resistance (R_s) values were determined from the fits of the tunneling current density expression as given in Eq. (2) to the measured J–V data set. The temperature dependences of $J_{s(\text{tunnel})}$ and E_{00} are shown in Fig. 3 and both $J_{s(\text{tunnel})}$ and R_s values in Table 1. It is evident that the saturation current shows weak temperature dependent behavior and the characteristic energy of tunneling shows temperature independent behavior in the temperature range 80–380 K. The results indicate that in this temperature range, the mechanism of the charge transport is performed by tunneling along dislocations intersecting the space charge region in the (Ni/Au)–AlN/GaN Schottky barrier diode [10–13].

The frequency-dependent capacitance and conductance were measured in a frequency range from 0.1 to 50 kHz in order to investigate the trapping effects in (Ni/Au)–AlN/GaN SBDs. The capacitance and conductance of the Schottky diode were measured simultaneously assuming a parallel combination of C and G. Fig. 4a and b shows the typical C_m–V and G_m/ω–V characteristics of (Ni/Au)–AlN/GaN SBDs measured at 0.7, 1, 2, and 3 kHz, respectively. As seen in Fig. 4a and b, the measured C–V and G/ω–V plots shows both voltage and frequency dependent behaviors. In the accumulation regions for a given bias voltage, the C and G/ω decrease with increase in frequencies due to the frequency dependent response

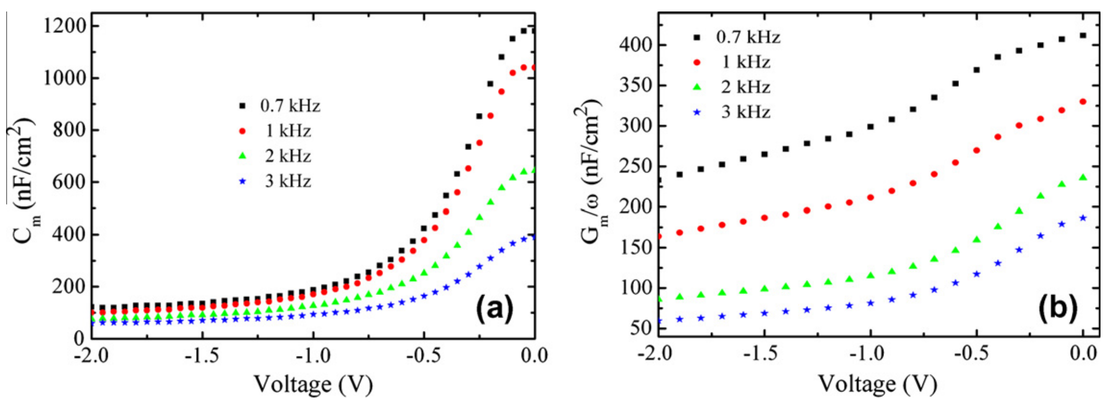

Fig. 4. (a) Typical measured capacitance and (b) conductance data as a function of voltage for (Ni/Au)–AlN/GaN SBDs measured at 0.7, 1, 2, and 3 kHz.

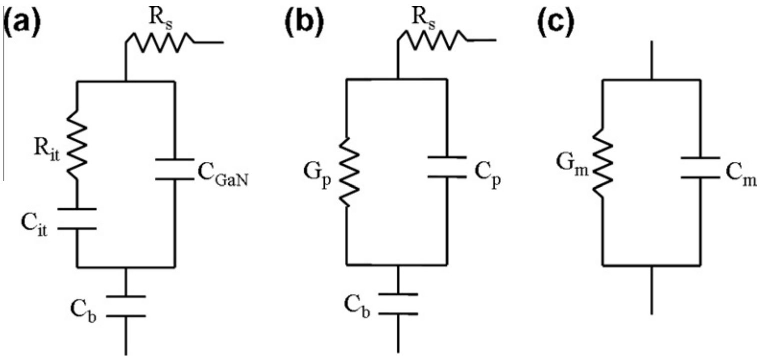

Fig. 5. Equivalent circuit model of (Ni/Au)–AlN/GaN SBDs used to extract trap parameters from the experimental measurements. (a) The measurement circuit, (b) the assumed model with interface traps states and (c) converted to the simplified circuit.

of interface states. At lower frequencies the interface states can follow the ac signal and yield a frequency dependent excess capacitance. In the high-frequency limit, however, the interface states cannot follow the alternating current (ac) signal. This makes the contribution of interface state capacitance to the total capacitance ignorable small [16,18].

The method described by Schroder for MOS capacitor analysis, which was adapted for the interface trap characterization of $Al_{0.15}Ga_{0.85}N$/GaN HFET structures by Miller et al. [15], was used in the interface trap investigation in (Ni/Au)–AlN/GaN SBDs [14–21]. There are four main possibilities to consider for the spatial location of traps in (Ni/Au)–AlN/GaN SBDs: (1) the metal–semiconductor interface of the Schottky contact, (2) the bulk of the barrier layer, (3) the interface between the barrier layer and the channel, and (4) the bulk of the channel layer [15,17,18,20]. It is impossible to know where the traps are located a priori; all four locations must be considered. Miller et al. [15] published a detailed and systematic analysis about the trap states investigation in $Al_{0.15}Ga_{0.85}N$/GaN HFET structures. They used the various models that account for the presence of the traps that are located at the heterojunction, in the bulk of the barrier layer and at the metal–semiconductor interface [15]. They measured the density and time constant of the trap states, but they could not determine the location of the traps unambiguously. In this study, the analysis of the frequency-dependent capacitance and conductance data was performed assuming models in which traps are present at the heterojunction-interface traps in our study.

The full circuit model in our analysis is shown in Fig. 5a, where C_b is the barrier capacitance (AlN layer), C_{GaN} is the capacitance of the GaN depletion region capacitor, R_s is the series resistance of the ohmic contact, and C_{it} and R_{it} are the interface trap capacitance and associated loss term for the traps. The full circuit in Fig. 5a can be shown by the simplified circuit of Fig. 5b. The capacitance and conductance of the Schottky barrier diode were measured simultaneously assuming a parallel combination of C and G, as shown in Fig. 5c.

The parallel conductance G_p/ω can be obtained from the measured C_m and G_m/ω curves by using the relation [14–16,21],

$$\frac{G_p}{\omega} = \frac{-\omega C_b^2(R_s C_m^2\omega^2 + R_s G_m^2 - G_m)}{\omega^4 C_m^2 C_b^2 R_s^2 + \omega^2(C_b^2 R_s^2 G_m^2 + C_m^2 + C_b^2 - 2C_b^2 R_s G_m - 2C_m C_b) + G_m^2} \quad (4)$$

In the equation, the barrier capacitance C_b was taken as the C_{AlN} capacitance values. In addition, R_s is the series resistance. The C_b value was determined from the plateau in the C–V curves that are associated with the accumulation of electrons in the two-dimensional electron gas channel. The C_b values used as 1600 nF/cm^2 were measured at 0.1 kHz. R_s and were calculated from the forward bias I–V characteristics in room temperature by fitting the tunneling current expression (Eq. (2)) to the experimental data (Table 1).

The G_p/ω as functions of frequency, by assuming a continuum of trap levels, can be expressed as [15,17],

$$\frac{G_p}{\omega} = \frac{qD_t}{2\omega\tau_t}\ln\left[1+\omega^2\tau_t^2\right] \quad (5)$$

Fig. 6 shows the calculated G_p/ω–ln(ω) curves of the AlN/GaN heterostructures for a different bias voltage. G_p/ω versus ln(ω) gives a peak for each bias voltage value due to the D_t contribution. The D_t and τ_t were calculated by fitting Eq. (5) to the experimental G_p/ω versus ln(ω) curves. By use of the appropriate technique, each value of applied bias voltage is converted into a surface potential corresponding to the Fermi level position within the band gap that we are probing [16,22]. This procedure was applied for several values of bias voltage.

Fig. 7 shows the extracted D_t and τ_t as a function of energy separation from the conduction-band edge ($E_c - E_t$). The resulting calculated parameters of the AlN/GaN HEMTs were $D_t \cong (5-8)\times 10^{12}$ eV^{-1} cm^{-2} and $\tau_t \cong (43-102)$ µs for the interface trap states, respectively.

Kordoš et al. [20] investigated the trapping effects in an Al_2O_3/AlGaN/GaN metal–oxide–semiconductor heterostructure field-effect transistor by temperature dependent conductance measurements. They identified two dominant trap states time constant as 1 µs and 10 ms and trap state density of the order of 10^{12} eV^{-1} cm^{-2}. On the other hand, Wu et al. [19] published a study on the electrical characterization of Al_2O_3/GaN interfaces

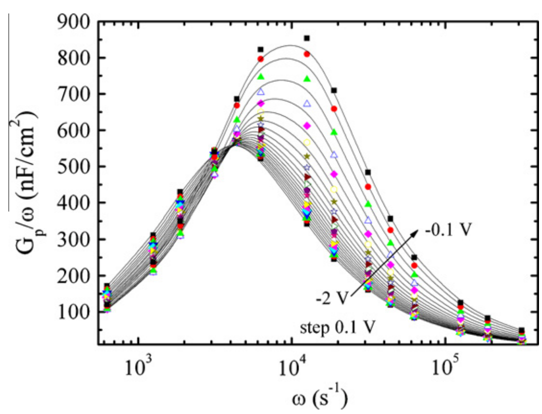

Fig. 6. Parallel conductance as a function of frequency for (Ni/Au)–AlN/GaN SBDs at different bias voltage values. The solid curves are the best fit of Eq. (5) to the experimental data.

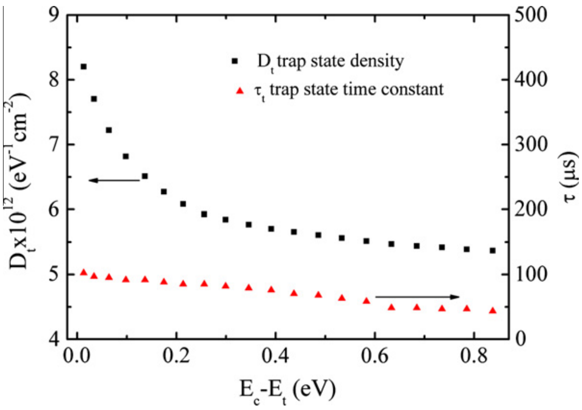

Fig. 7. Experimentally derived density (D_t) and time constants (τ_t) of the trap states as a function of energy separation from the conduction-band edge ($E_c - E_t$) for (Ni/Au)–AlN/GaN SBDs.

by photo-assisted capacitance–voltage characterization. They report the average interface trap density D_{it} of $(1\text{–}2) \times 10^{12}$ eV^{-1} cm^{-2}. In this study, our measured trap state density and time constant ($D_t \cong (5\text{—}8)1 \times 10^{12}$ eV^{-1} cm^{-2} $\tau_t \cong (43\text{—}102)$ μs) are consistent with the reported results for the GaN based structures.

4. Conclusions

The mechanism of charge transport in the (Ni/Au)–AlN/GaN Schottky barrier diodes were investigated by the use of current–voltage characteristics in the temperature range of 80–380 K. The true current transport mechanisms for (Ni/Au)–AlN/GaN SBDs were determined by fitting the analytical expressions given for the current transport mechanisms to the experimental *J*–*V* data in a wide range of applied biases and at different temperatures, by taking the $J_{s(\text{tunnel})}$, E_0, and R_s as adjustable fit parameters. Fitting results show the weak temperature dependent behavior in the saturation current and the temperature independent behavior of the tunneling parameters in this temperature range. Therefore, it has been concluded that the mechanism of charge transport in (Ni/Au)–AlN/GaN SBDs, along the dislocations intersecting the space charge region, is performed by tunneling.

Furthermore, in order to investigate the trapping effects in AlN/GaN heterostructures, the frequency dependent (*C*–*V*) and (*G*/ω–*V*) measurements were done in the frequency range 0.7–50 kHz. A detailed analysis of the frequency-dependent capacitance and conductance data was performed, assuming the models in which traps are located at the heterojunction interface. The density (D_t) and time constants (τ_t) of the trap states have been determined as a function of energy separation from the conduction-band edge ($E_c - E_t$) as $D_t \cong (5\text{—}8) \times 10^{12}$ eV^{-1} cm^{-2} and $\tau_t \cong (43\text{—}102)$μs, respectively.

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References

[1] Mohammad SN, Salvador A, Morkoç H. Proc IEEE 1995;83:1306.
[2] Arslan Engin, Öztürk MustafaK, Duygulu Özgür, Kaya AliArslan, Özçelik Süleyman, Özbay Ekmel, et al. Mater Sci Process 2009;94:73.
[3] Kuzmík J, Kostopoulos A, Konstantinidis G, Carlin J-F, Georgakilas A, Pogany D. IEEE Trans Electron Dev 2006;53:422.
[4] Medjdoub F, Carlin J-F, Gonschorek M, Feltin E, Py MA, Ducatteau D, et al. Tech Dig-Int Electron Dev Meet 2006:1.
[5] Cao Y, Wang K, Orlov A, Xing H, Jena D. Appl Phys Lett 2008;92:152112.
[6] Elsass CR, Smorchkova IP, Heying B, Haus E, Fini P, Maranowski K, et al. Appl Phys Lett 1999;74:3528. MBE ALGAN/&GAN HEMT.
[7] Binari SC, Doverspike K, Kelner G, Dietrich HB, Wickenden AE. Solid-State Electron 1997;41:177.
[8] Alekseev E, Eisenbach A, Pavlidis D. Electron Lett 1999;35:2145.
[9] Sze SM. Physics of semiconductor devices. 2nd ed. New York: John Wiley&Sons; 1981.
[10] Arslan Engin, Altındal Şemsettin, Özçelik Süleyman, Ozbay Ekmel. Semicond Sci Technol 2009;24:075003.
[11] Arslan Engin, Altındal Şemsettin, Özçelik Süleyman, Ozbay Ekmel. J Appl Phys 2009;105:023705.
[12] Belyaev AE, Boltovets NS, Ivanov VN, Klad'ko VP, Konakova RV, Kudrik Ya Ya, et al. Semiconductors 2008;42:689.
[13] Evstropov VV, Dzhumaeva M, Zhilyaev YuV, Nazarov N, Sitnikova AA, Fedorov LM. Semiconductors 2000;34:1305.
[14] Schroder DK. Semiconductor material and device characterization. 3rd ed. Hoboken, NJ: Wiley; 2006.
[15] Miller EJ, Dang XZ, Wieder HH, Asbeck PM, Yu ET, Sullivan GJ, et al. J Appl Phys 2000;87:8070.
[16] Nicollian EH, Brews JR. MOS (metal/oxide/semiconductor) physics and technology. New York: John Wiley&Sons; 1982.
[17] Stoklas R, Gregušová D, Novák J, Vescan A, Kordoš P. Appl Phys Lett 2008;93:124103.
[18] Chu RM, Zhou YG, Chen KJ, Lau KM. Phys Status Solidi (C) 0, 2400 (2003).
[19] Wu YQ, Shen T, Ye PD, Wilk GD. Appl Phys Lett 2007;90:143504.
[20] Kordoš P, Stoklas R, Gregušová D, Gaži Š, Novák J. Appl Phys Lett 2010;96:013505.
[21] Nicollian EH, Goetzberger A. Bell Syst Tech J 1967;46:1055.
[22] Shenoy JN, Shindalore GL, Melloch MR, Cooper Jr JA. J Electron Mater 1995;24:303.