Research Article

SURFACE and INTERFACE ANALYSIS

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Temperature-dependent profile of the surface states and series resistance in (Ni/Au)/AlGaN/AlN/GaN heterostructures†

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The profile of the interface state densities (N_{ss}) and series resistances (R_s) effect on capacitance–voltage ($C-V$) and conductance-voltage ($G/\omega-V$) of (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN heterostructures as a function of the temperature have been investigated at 1 MHz. The admittance method allows us to obtain the parameters characterizing the metal/semiconductor interface phenomena as well as the bulk phenomena. The method revealed that the density of interface states decreases with increasing temperature. Such a behavior of N_{ss} can be attributed to reordering and restructure of surface charges. The value of series R_s decreases with decreasing temperature. This behavior of R_s is in obvious disagreement with that reported in the literature. It is found that the N_{ss} and R_s of the structure are important parameters that strongly influence the electrical parameters of (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN($x = 0.22$) heterostructures. In addition, in the forward bias region a negative contribution to the capacitance C has been observed, that decreases with the increasing temperature. Copyright © 2010 John Wiley & Sons, Ltd.

Keywords: (Ni/Au)/AlGaN/AlN/GaN heterostructures; interface states; negative capacitance; frequency dependence; series resistance

Introduction

The performance and reliability of electronic devices such as metal–semiconductor (MS), metal–insulator–semiconductor (MIS), metal–ferroelectric–semiconductor (MFS) or metal–ferroelectric–insulator–semiconductor (MFIS), metal–oxide–semiconductor field effect transistor (MOSFET) and high electron mobility transistors (HEMTs) are dependent especially on the formation barrier height at M/S interface, and series resistance (R_s) of devices, doping concentration and density of interface states (N_{ss}).[1–6] Also, change in temperature has very important effects on the parameters of such devices.[7–9] The existence of an interfacial insulator layer at M/S interface and the R_s of the device significantly alter the device's capacitance–voltage ($C-V$) and conductance–voltage ($G/\omega-V$) characteristics. In recent years, some investigations have reported a negative capacitance (NC)[1,2,4,5,10–12] in the forward bias $C-V$ characteristic. The term NC means that the material displays an inductive behavior. The observation of NC is important because it implies that an increment of bias voltage produces a decrease in the charge on the electrodes.[4] However, NC has, so far, no meaning to us and the concept of NC is still not widely recognized because of lack of trust in experimental data.[12] Therefore, in many cases experimental NC data were not reported in the literature due to confusion caused by the NC effect.[13] Practically, NC can be explained based on the behavior of temperature and frequency dependent admittance spectroscopy ($C-V$ and $G/\omega-V$) data.[12] As the electrons that surmount the Schottky barrier (SB) under forward bias do fill up the empty states at the interface and possess excess energy, when colliding with the electrons trapped at the N_{ss} they could also knock electrons out of the traps, provided the binding energy of these traps is smaller than the SB energy.[2,13]

Both the N_{ss} and R_s values of these devices are important parameters that affect the main electrical parameters.[14] Since a bias voltage is applied across these structures, the combination of the interfacial insulator layer, depletion layer and series resistance of the device will share the applied bias voltage. The N_{ss} and bulk traps formed at M/S interface, where charges can be stored and released when the appropriate forward applied bias and the external a.c. oscillation voltage are applied, strongly affect device performance.[1,2,4,5,11] Although it is believed that the injection of charge carriers involves a process of hopping to localized interface traps, a detailed physical mechanism of injection is not yet understood.

In this study, the origin of NC in the forward bias $C-V$ characteristics of (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN($x = 0.22$) heterojunctions has been investigated between 80 and 400 K at 1 MHz. Experimental results show that the value of NC decreases with increasing temperature at forward bias voltage and this decrease corresponds to an increase of the conductance. In addition, the temperature-dependent profiles of N_{ss} and R_s were found at each temperature by using the Hill–Coleman[15] and conductance[16] methods, respectively.

Experimental

The $Al_xGa_{1-x}N$/AlN/GaN ($x = 0.22$) heterostructures were grown on a double-polished 2-inch diameter (0001) sapphire (Al_2O_3) substrate in a low pressure Metal-Organic Chemical-Vapor Deposition

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(MOCVD) reactor (Aixtron 200/4 HT-S) by using trimethylgallium (TMGa), trimethylaluminum (TMAl), and ammonia as Ga, Al, and N precursors, respectively. Prior to the epitaxial growth, Al_2O_3 substrate was annealed at 1100 °C in a high vacuum under a pressure of 10^{-7} Torr for 10 min in order to remove surface contamination. In order to design AlGaN/AlN/GaN heterojunction structures, we have grown GaN, AlN and AlGaN layers on a sapphire substrate. Because of large lattice and thermal mismatch we used buffer layers between substrate and GaN layer. In AlGaN/AlN/GaN heterojunction, the AlGaN, AlN and GaN layers are the barrier, spike and buffer layers, respectively. The buffer structures consisted of a 15-nm-thick, low-temperature (650 °C) AlN nucleation layer and high-temperature (1150 °C) 420-nm AlN templates. A 1.5-µm nominally undoped GaN layer was grown on an AlN template layer at 1050 °C, followed by a 2-nm-thick high-temperature AlN (1150 °C) barrier layer. After the deposition of these layers, a 23-nm-thick undoped $Al_{0.22}Ga_{0.78}N$ layer was grown on an AlN layer at 1050 °C. Finally, a 5-nm-thick GaN cap layer growth was carried out at a temperature of 1085 °C and a pressure of 50 mbars.

The ohmic contacts were formed as a square van de Pauw shape and the Schottky contacts formed as 1 mm diameter circular dots.[17] Prior to ohmic contact formation, the samples were cleaned with acetone in an ultrasonic bath. Then, the sample was treated with boiling isopropyl alcohol for 5 min and rinsed in deionized (DI) water having 18 MΩ resistivity. After cleaning, the samples were dipped in a solution of HCl/H_2O (1 : 2) for 30 s in order to remove the surface oxides and then rinsed in DI water again for a prolonged period. Ti/Al/Ni/Au (17.5/175/40/150 nm) metals were thermally evaporated on the sample and annealed at 850 °C for 30 s in ambient N_2 in order to form the ohmic contact. In order to obtain a rectifying/Schottky contacts, Ni/Au (40/80 nm) layer was coated on the top of sample in the high vacuum coating system at about 10^{-7} Torr. The schematic diagram of (Ni–Au)/AlGaN/AlN/GaN heterostructures has been already published.[17]

The C–V–T and G/ω–V–T measurements of the (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN($x = 0.22$) heterostructures were taken using a computer controlled HP 4192 A LF impedance analyzer at 1 MHz. The sample temperature was controlled using Janes vpf-475 cryostat, which enables us to take measurements in the temperature range of 77–450 K. Also, the sample temperature was continually monitored by using a copper-constant thermocouple close to the sample and measured with a Keithley model 199 DMM/scanner and a Lake Shore model 321 auto-tuning temperature controller with sensitivity better than ±0.1 K.

Results and Discussion

It is well known that the analysis of the C–V and G/ω–V characteristics of semiconductor devices such as MS, MIS, MOS and HEMTs only at room or narrow temperature range cannot give us detailed information about the main electrical parameters and/or conduction mechanisms. However, the C–V and G/ω–V measurements of these devices in the wide temperature and bias voltage regions allows us to understand different aspects of conduction mechanisms or the temperature and bias voltage dependence behavior of main electrical parameters. Therefore, we have investigated the C–V and G/ω–V characteristics of (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN($x = 0.22$) heterostructures in the wide temperature range of 80–400 K and at 1 MHz. Figure 1(a) and (b) shows the plots of the measured C–V and G/ω–V of (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN heterostructure in the temperature range 80–400 K.

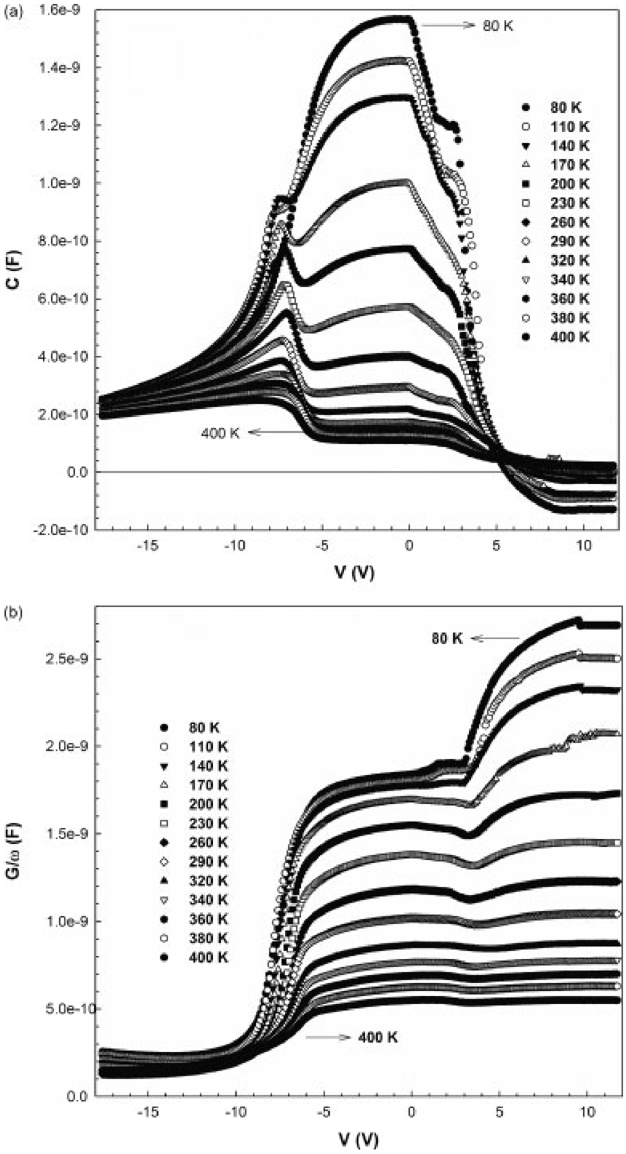

Figure 1. The temperature-dependent plots of (a) the C–V and (b) G/ω–V characteristics for the (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN heterostructure measured at 1 MHz.

As shown in Fig. 1(a) and (b), both the values of C and G/ω decrease with increasing temperature especially in the accumulation and depletion regions for each bias voltage. In addition, an interesting feature of the forward bias C–V curves is the nearly common intersection point (at about 5.5 V) of all the curves at a certain bias voltage, and for this voltage point, the conduction through the junction is temperature independent. The intersection behavior of the C–V curves appears abnormal when compared to the conventional behavior of ideal Schottky diodes and MIS structures. This behavior is attributed to the lack of free charge at low temperature and in the region, where there is no carrier freezing out, which is nonnegligible at low temperature, in particular. On the other hand, the existence of R_s in these structures causes bending due to charge saturation, and plays a subtle role in keeping this intersection hidden.[14] When the temperature is increased, the generation of thermal carriers (electrons or holes) in semiconductor is enhanced both at positive and negative biased conditions. Therefore, the increase of C with the temperature for

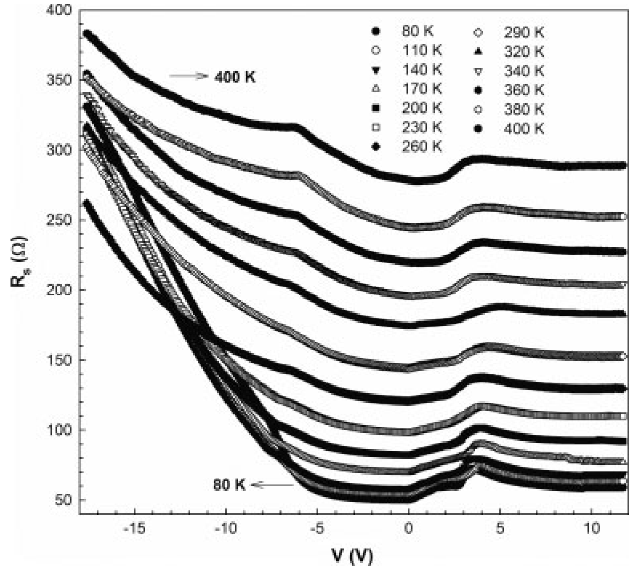

Figure 2. The temperature-dependent R_s for the (Ni/Au)/Al$_x$Ga$_{1-x}$N/AlN/GaN heterostructure measured at 1 MHz.

Table 1. The values of different parameters for a (Ni/Au)/Al$_x$Ga$_{1-x}$N/AlN/GaN heterostructure determined from C–V and G/ω–V characteristics in the temperature range 80–400 K

T (K)	$V_{\max}$ (V)	$C_{\max}$ (F)	$(G_m/\omega)_{\max}$ (F)	N_{ss} (eV^{-1} cm^{-2})
80	−7.9	7.06E−10	8.11E−10	1.76E+12
110	−7.7	9.10E−10	9.94E−10	2.38E+12
140	−7.4	9.50E−10	1.05E−09	2.56E+12
170	−7.3	8.50E−10	9.85E−10	2.29E+12
200	−7	7.60E−10	9.30E−10	2.07E+12
230	−7.1	6.50E−10	7.05E−10	1.49E+12
260	−6.9	5.48E−10	6.36E−10	1.28E+12
290	−7.1	4.50E−10	5.39E−10	1.04E+12
320	−7.2	3.82E−10	4.42E−10	8.29E+11
340	−7.4	3.43E−10	3.79E−10	6.99E+11
360	−7.5	3.07E−10	3.45E−10	6.27E+11
380	−7.6	2.78E−10	3.20E−10	5.74E+11
400	−7.8	2.46E−10	3.03E−10	5.36E+11

all applied bias levels can be understood due to charge storage (= Q/V). The other interesting feature, as can be seen in Fig. 1(a), is that the values of capacitance give two peaks. The first peak in the depletion region due to interface states (N_{ss}) contribution shifts from the negative bias voltage to the forward bias voltage as the temperature increases. However, the second peak shown in the accumulation region disappears when the temperature increases. Such a behavior of the second peak is due to the influence of the series resistance (R_s) of the heterostructures. While the values of N_{ss} are effective especially in the depletion and weak inversion regions, the values of R_s are effective only in the accumulation region.

In addition, C–V–T curves show negative values after a certain forward bias voltage (∼5.5 V). Contrary to the C–V curves, the values of G/ω increase from the inversion region to the strong accumulation region at each temperature. As shown in Fig. 1(a) and (b), the NC values appear especially at low temperatures ($T \leq 260$ K) and at high temperatures ($T > 260$ K) they disappear. Also, as can be seen in Fig. 1(b), the NC values correspond to the maximum of the device conductance. Such a behavior of C–V–T and G/ω–V–T shows that the material displays an inductive behavior.[11,12] It is believed that the injection of charge carriers involves a process of hopping to localized interface traps/states, but detailed physical mechanisms of injection are not yet understood.

Temperature dependence of R_s can be determined from the measurements of C–V–T and G/ω–V–T curves at sufficiently high frequency as[16]

$$R_s = \frac{G_m}{G_m^2 + (\omega C_m)^2} \qquad (1)$$

where C_m and G_m represent the measured capacitance and conductance for any bias voltage, respectively. Figure 2 shows the variation of the series resistance as a function of temperature. These very significant values demand that special attention should be given to effect of the R_s in the application of the frequency and temperature-dependent C–V and G/ω–V measurements. It is clearly seen in Fig. 2 that the values of R_s decrease with the increasing bias voltage from strong inversion region to accumulation region. Also, the values of R_s increase with increasing temperature both in the accumulation and depletion regions. Such a temperature dependence of R_s is in obvious disagreement with the reported negative temperature coefficient of the ideal Shottky barrier diodes (SBDs) and MIS type SBDs. Similar results have been reported in the literature.[18] This change in the R_s with the temperature can be expected for semiconductors in the temperature region where there is no freezing behavior of the carriers. We believe that the trap charges have sufficient energy to escape from the traps that are located between the metal and semiconductor interface.

It is well known that the density of interface states (N_{ss}) is a useful guide for the quality of semiconductor devices such as SBDs and HEMTs structures. There are several methods to determine N_{ss}.[15,16,19] Among them, Hill–Coleman method[15] is important in terms of being fast and reliable. According to this method, density of interface states can be expressed as

$$N_{ss} = \frac{2}{qA} \frac{(G_m/\omega)_{\max}}{((G_m/\omega)_{\max} C_{ox})^2 + (1 - C_m/C_{ox})^2}, \qquad (2)$$

where A is the area of rectifier contact, ω is the angular frequency, C_m and $(G_m/\omega)_{\max}$ are the measured capacitance and conductance which correspond to the peak values, respectively, and C_{ox} is the capacitance of insulator layer. The values of various parameters for a (Ni/Au)/Al$_x$Ga$_{1-x}$N/AlN/GaN heterostructure determined from C–V and G/ω–V characteristics in the temperature range of 80–400 K are given in Table 1 and Figs (3) and (4), respectively.

As shown in Figs (3) and (4) the values of $C_{\max}$, $G/\omega_{\max}$ and N_{ss} give a peak at about 140 K. This is a result of molecular restructuring and reordering of the metal–semiconductor interface caused by the temperature.[20]

Conclusions

The temperature-dependent profiles of the N_{ss} and R_s were obtained from forward and reverse bias C–V–T and G/ω–V–T characteristics of (Ni/Au)/Al$_x$Ga$_{1-x}$N/AlN/GaN($x = 0.22$) heterostructures in the wide temperature range of 80–400 K at 1 MHz.

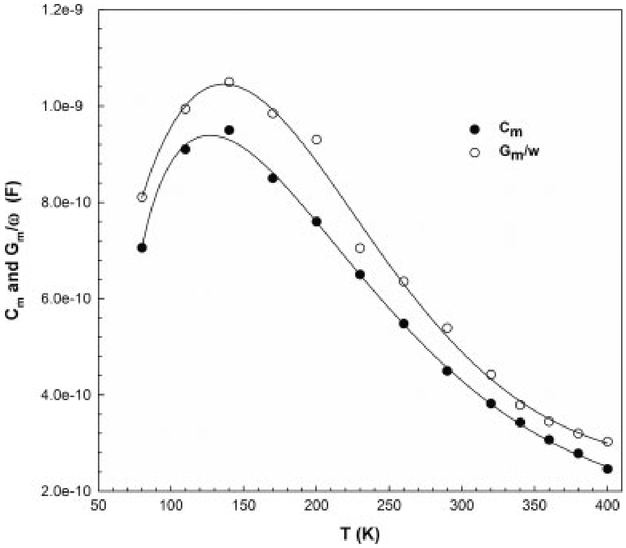

Figure 3. The variation of the C_{max} and $(G_m/\omega)_{max}$ for (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN heterostructures as a function of the temperature at 1 MHz.

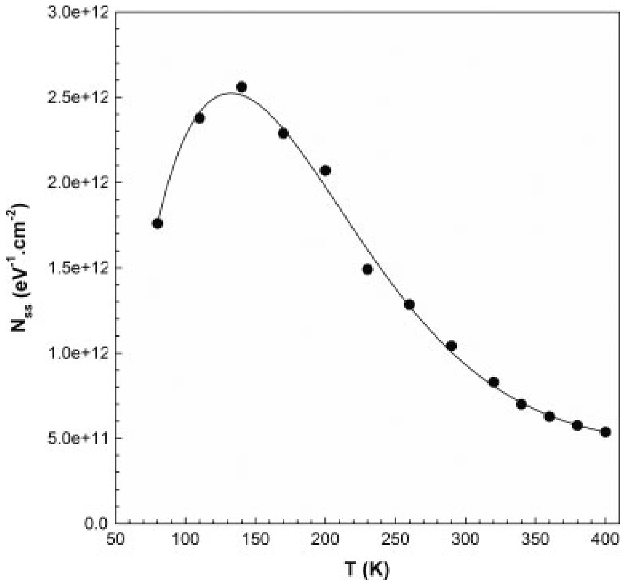

Figure 4. The variation of the N_{ss} for (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN heterostructures as a function of the temperature at 1 MHz.

It was found that both the C and G/ω were quite sensitive to temperature, especially at relatively low temperature. The value of series R_s decreases with decreasing temperature. This behavior of R_s is in obvious disagreement with that reported in literature The value of N_{ss} gives a peak at about 140 K due to molecular restructuring and reordering of the interface states and dislocations between the metal and the semiconductor. In addition, the $C-V$ plots cross at certain forward bias voltage points (~5.5 V) and then show negative values. The intersection behaviors of $C-V$ curves and the increase in R_s with temperature were attributed to the lack of free charge especially at a low temperature. The value of NC decreases with increasing temperature at forward bias voltage and this decrease of the NC corresponds to an increase of the conductance. It is thought that the capacitance value decreases with increasing polarization and more carriers are introduced in the structure. It is found that the N_{ss} and R_s of the structure are important parameters that strongly influence the electrical parameters of (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN heterostructures.

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