## Fabrication of 200-GHz $f_{max}$ Resonant-Tunneling Diodes for Integrated Circuit and Microwave Applications

## S. K. DIAMOND, E. ÖZBAY, M. J. W. RODWELL, DAVID M. BLOOM, FELLOW, IEEE, Y. C. PAO, E. WOLAK, AND JAMES S. HARRIS, FELLOW, IEEE

Abstract—Room-temperature current densities of  $1.3 \times 10^{5}$  A/cm<sup>2</sup> and peak-to-valley ratios of 2.5 have been achieved for resonant tunneling diodes (RTD's) in the GaAs/AlAs material system. The devices were fabricated in a microwave-compatible process employing topside contacts and a semi-insulating substrate to allow device integration. Proton implantation creates a nonconducting surface compatible with highfrequency coplanar transmission lines and other passive microwave structures.

**F**OR resonant-tunneling diodes (RTD's), the charging time constant of the device capacitance eventually limits highfrequency operation. For this reason, high-current and lowcapacitance devices can be equated with high-speed devices. Fabricating discrete devices, Brown *et al.* have demonstrated RTD's with current densities in excess of  $4 \times 10^4$  A/cm<sup>2</sup> and capacitances less than 1.6 fF/ $\mu$ m<sup>2</sup> [1]. These devices have demonstrated high-frequency operation, with maximum oscillation frequencies above 200 GHz, however fabrication methods have been unsuitable for the integration of devices.

For circuit applications such as parity-bit generation, frequency dividers, and binary and multilevel logic circuits it is necessary integrate several devices in simple circuit configurations. To date, this has been achieved in the growth process, with several double-barrier structures grown sequentially on top of each other. This has resulted in circuits which have demonstrated the desired functionality, however, the current densities achieved have been less than  $3 \times 10^3$  A/cm<sup>2</sup> and high-frequency operation has not been attained [2], [3]. If devices are properly isolated then this integration can be easily accomplished on chip by a series connections of devices with no corresponding complexities in growth.

Microwave integrated circuit applications such as mixers, frequency multipliers, and pulse-forming circuits require onchip integration of high-quality transmission lines as well as possible integration of filters, inductors, and other passive microwave elements. This necessitates the use of a low-loss

Y. C. Pao, E. Wolak, and J. S. Harris are with the Department of Electrical Engineering, Stanford University, Stanford, CA 94305.

IEEE Log Number 8926653.

nonconducting substrate to serve as the dielectric of transmission lines. The common practice of placing metal interconnections on nitride layers over conducting material results in structures with high loss and high capacitance, unsuitable for high-frequency operation.

In this letter, we demonstrate a fabrication process which produces high-quality RTD's, with a maximum frequency of oscillation above 200 GHz, in a process suitable for integration of devices and suitable for microwave structures.

The device material used for the present work was grown by molecular beam epitaxy in a Varian GEN II on a 2-in (100) semi-insulating GaAs substrate. A  $0.9-\mu m 1 \times 10^{18} n^+$  Sidoped layer was grown to provide the bottom ohmic contact. A 700-Å undoped GaAs spacer layer was grown on top of this, followed by the RT double barrier. The latter consists of a 16-monolayer GaAs well sandwiched between two 6monolayer AlAs barriers. This was followed by a shorter 100-Å undoped spacer layer and a  $0.45-\mu m 1 \times 10^{18}$  doped top ohmic contact. The growth rate was  $0.8 \ \mu m/h$  for GaAs with an As-to-Ga ratio of 16. To ensure uniformity, the substrate was rotated at 20 rpm, and 20-s growth interruptions were used at the heterointerfaces.

A semi-insulating substrate was used to allow for device isolation and the fabrication of low-parasitic interconnections and low-loss transmission lines. Asymmetric spacer layers are used with the device. A 100-Å cathode spacer layer was chosen to minimize the accumulation layer formation on the emitter side [5]. For anode spacer layers less than 1000 Å thickness, the spacer layer allows a trade-off between minimizing device capacitance and maximizing device negative conductance, while maintaining the  $R_n C$  product constant [4]. For switching applications it is the product  $R_n C$  which determines switching transition times. By varying the spacer thickness the negative differential resistance  $R_n$  can be varied without affecting switching speed. For these devices, a long 700-Å spacer layer was chosen to ensure that the device negative resistance would be larger than the (spacer independent) series resistance from the ohmic contacts and epi layers. The thick spacer may also be partially responsible for the unusually high peak-to-valley current ratios (PVR's) and current densities obtained. Due to the lack of dopants, highquality GaAs is obtained prior to barrier growth, and fewer scattering centers may be incorporated in the barriers.

The previously discussed requirements for high-speed integratable RTD's were achieved with a four-step masking process resulting in a stripe geometry RTD structure as shown

Manuscript received October 31, 1988; revised December 9, 1988. This work was supported by the Office of Naval Research under Contract N00014-86-K-0530.

S. K. Diamond, E. Özbay, and D. M. Bloom are with the Edward L. Ginzton Laboratory, Stanford University, Stanford, CA 94305.

M. J. W. Rodwell was with the Edward L. Ginzton Laboratory, Stanford University, Stanford, CA 94305. He is now with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106.



Fig. 1. SEM microphotograph of stripe-geometry RTD design. The long narrow stripe is the top ohmic contact. On either side are bottom ohmic contacts. Interconnect metallization is used to connect the device to a bond pad compatible with microwave wafer probes.



Fig. 2. Device cross section of proton-implanted, microwave-compatible RTD process. Proton isolation provides an nonconducting low-loss dielectric for transmission lines and device isolation.

in the SEM microphotograph of Fig. 1 and the device cross section of Fig. 2. Initially, two rectangular holes are etched down to the bottom n<sup>+</sup> region and Ni/Ge/Au is deposited for the bottom ohmic contact. The etch serves to define the RTD active region in one dimension. Ni/Ge/Au is then deposited on the narrow island formed between the two previously etched holes to form the top ohmic, and the contacts are annealed at 450°C for 20 s. Definition of the active area in the other dimension, device isolation, and rendering of the GaAs nonconducting is achieved through proton isolation. The proton isolation step consists of masking the top ohmic contact and the majority of the bottom ohmic with 1  $\mu$ m of polyimide followed by 1.6  $\mu$ m of Au. Protons are then implanted at 30, 90, and 190 keV with dosages of  $1.0 \times 10^{14}$ ,  $1.7 \times 10^{14}$ , and  $5.6 \times 10^{14}$  atoms/cm<sup>2</sup>, respectively. Ti/Au metallization can now be deposited directly on the GaAs and devices can now be connected with "random" wiring as in digital circuits or with coplanar transmission lines. Other passive microwave structures may also be incorporated at this step.



Fig. 3 Static I-V curves for typical devices at room temperature and 77 K

The series resistance of the bottom ohmic contacts and the bottom  $n^+$  layer is inversely proportional to the device perimeter, thus devices were fabricated in a stripe geometry. In addition, unlike standard RTD's with frontside and back-side wafer contacts, with these devices there is a lateral current flow and there can be a substantial difference in applied voltage between the center and edge of the RTD active area for stripe widths greater than 10  $\mu$ m. For this reason, the lateral width is kept as small as possible within processing constraints (= 5  $\mu$ m), and large area devices are made by extending the stripe length.

Fig. 3 shows typical room-temperature and 77 K static current-voltage (I-V) characteristics. The devices exhibit current densities in the range of  $0.9-1.3 \times 10^5$  A/cm<sup>2</sup> with PVR's from 2 to 2.5. At 77 K, current densities increase to  $1.5-1.7 \times 10^5$  A/cm<sup>2</sup> with PVR's from 5.2 to 6.1. These devices are unique, for the GaAs/AlAs system, in their high current densities and simultaneous high PVR's.

Essential to any circuit application is an accurate circuit model and well-characterized circuit properties. The proposed small-signal equivalent circuit for RTD's is a resistance  $R_{1}$  in series with the parallel combination of a capacitance C and a voltage dependent resistance  $R_n$  [1].  $R_n$  can actually be positive or negative depending on the bias point. For this device geometry, the series resistance is estimated at 230  $\Omega \cdot \mu m^2$  from on-wafer measurements of contact resistance, known values of GaAs resistivity, and measured ohmic contact line widths and spacings. The capacitance is estimated as  $\epsilon A/d$ where d is the combined thickness of the 700-Å undoped spacer layer and 70- Å well region thickness. This results in a device capacitance of 1.3 fF/ $\mu$ m<sup>2</sup>. Because of the high doping outside of the spacer layer, this capacitance should be relatively independent of bias voltage. It is apparent from the static I-V curves that the device oscillates when biased in the negative differential resistance region and thus is it not possible to ascertain the maximum negative conductance. However, the average negative differential resistance over the entire negative resistance region can be obtained as  $R_n^{avg}$  =  $(V_{\text{peak}} - V_{\text{valley}})/(I_{\text{peak}} - I_{\text{valley}}) - R_s$ . For these devices this results in  $R^{avg} = -650 \ \Omega \cdot \mu m^2$ .

To test the RTD equivalent circuit and check our estimates for circuit parameters, a number of the devices were connected to bond pads compatible with microwave wafer probes. This bond pad introduced an additional parasitic capacitance of 32 fF across the device.  $S_{11}$  measurements were made from 45 MHz to 26.5 GHz for several bias voltages. Unfortunately, even the smallest devices had negative impedances less than 50  $\Omega$  and therefore oscillate when measured in a 50- $\Omega$  system, and  $S_{11}$  could not be measured in the negative resistance region. At other bias points,  $S_{11}$  was measured,  $R_n$  was estimated from the static I-V curve, and the  $S_{11}$  values of the equivalent circuit (including the effect of the pad capacitance) were calculated and compared with the measured data. The calculated  $S_{11}$  values closely tracked the measured data.

To measure the large-signal switching performance of these devices, voltage step forming structures were fabricated. The structure consists of a 50- $\Omega$  coplanar transmission line. At the midpoint of the line a RTD is connected in shunt from the center conductor of the line to ground. In this test structure, reflections from the bond-pad capacitance at the line endpoints are separated in time from the RTD switching transients and hence do not degrade the measured switching time. A few gigahertz sine wave is applied to the input transmission line. The input amplitude is sufficient to switch the RTD from a voltage less than resonance to one past resonance. As the device switches, a voltage step travels down the transmission lines. Switching measurements were tried with  $25 - \mu m^2$  devices which had an average negative resistance of 26  $\Omega$  and a series resistance of 9.2  $\Omega$ . With the parallel combinations of transmission lines, the effective load impedance was 34.2  $\Omega$ (25 + 9.2). An analysis of switching transition times for this value of load impedance and negative resistance predicts switching times of  $10R_nC = 8.5 \text{ ps}$  [4]. The RTD voltage was measured at the RTD by electro-optic sampling [6]. Measured switching times were of the order of 10 ps. With an optimal load resistance across the device, the minimum obtainable rise time should be  $4.5R_nC = 3.8 \text{ ps}$ . Structures with a more appropriate load are currently being fabricated.

While oscillator structures were not fabricated on wafer, the maximum frequency of oscillation  $f_{max}$  can be calculated

$$f_{\max} = \frac{1}{2\pi |R_n|C} \sqrt{\frac{|R_n|}{R_s} - 1} = 250 \text{ GHz}$$
(1)

where  $|R_n^{avg}|$  was used for  $|R_n|$ .

In summary, we have fabricated resonant-tunneling diodes with high current densities and high  $f_{max}$ . The process results in isolated devices and low-loss transmission-line interconnections. Millimeter-wave RTD integrated circuits and highspeed RTD logic circuits can thus be fabricated.

## ACKNOWLEDGMENT

The authors wish to thank B. Park for useful discussions and K. Lear for assistance in process design and helpful discussions.

## References

- E. R. Brown, W. D. Goodhue, and T. C. L. G. Sollner, "Fundamental oscillations up to 200 GHz in resonant tunneling diodes and new estimates of their maximum oscillation frequency from stationary-state tunneling theory," J. Appl. Phys., vol. 64, pp. 1519-1529, 1988.
  R. C. Potter et al., "Three-dimensional integration of resonant
- [2] R. C. Potter et al., "Three-dimensional integration of resonant tunneling structures for signal processing and three-state logic," Appl. Phys. Lett., vol. 52, pp. 2163-2165, 1988.
- [3] S. Sen, F. Capasso, D. Sivco, and A. Y. Cho, "New resonant tunneling devices with multiple negative resistance regions and high room-temperature peak-to-valley ratio," *IEEE Electron Device Lett.*, vol. 9, pp. 402-404, 1988.
- [4] S. K. Diamond et al., "Resonant tunneling diodes for switching applications," Appl. Phys. Lett., vol. 54, pp. 153-155, 1989.
- [5] H. Ohnishi, T. Inata, S. Muto, N. Yokoyama, and A. Shibatomi, "Self-consistant analysis of resonant tunneling current," Appl. Phys. Lett., vol. 49, pp. 1248-1250, 1986.
- [6] K. J. Weingarten, M. J. W. Rodwell, and D. M. Bloom, "Picosecond optical sampling of GaAs integrated circuits," *IEEE J. Quantum Electron.*, vol. 24, pp. 198-220, Feb. 1988.